## REMARKS

In the Official Action mailed 16 October 2009, the Examiner reviewed claims 2, 5 and 7-18. The Examiner has withdrawn his previous rejections and has accepted and recorded the Terminal Disclaimer to US 6,453,446. The Examiner has rejected claims 2, 5 and 7-18 under 35 U.S.C. §102(b).

Applicant has amended claim 2. Claims 2, 5 and 7-18 remain pending.

The rejection is respectfully traversed below, and reconsideration is requested.

Rejection of Claims 2, 5 and 7-18 under 35 U.S.C. §102(b)

The Examiner has rejected claims 2, 5 and 7-18 under 35 U.S.C. §102(b) as being anticipated by Kannan *et al. A Methodology and Algorithms for Post-Placement Delay Optimization*, ACM, 31st ACM/IEEE Design Automation Conference, 1994, pp. 327-332.

Reconsideration is requested.

Kannan *et al.* does not describe step (c) in claim 2, including the elements:

1. "performing a placement… after determining said delay values…"
2. "determining size or area … in response to said assigned loads and said delay values."

Note that because of step (c) in the claim, the step (b) of "determining delay values …" must occur before the placement.

Applicant notes that the "delay values" for the cells as the term is used in the present application, are determined prior to placement, as a function of the inter-related values of delay due to the cell and the delay due to load of a placed cell. This interpretation of "delay values" is inherent in the language of the claim. As taught in the present application, once a load is assigned during placement to a cell, the size or area of the cell can be determined that is necessary to provide the drive power to achieve the delay target. The present invention determines delay values before placement as a function of delay to be provided by the cell and delay to be provided by the load. During placement, a load is assigned to the cell. Given the load assigned to the cell, and given the delay value set before placement, the cell size or area can be determined that is needed to achieve that delay value. Kannan *et al.* does not disclose the relationship stated in the claim, among determining the delay values, performing placement in which loads are assigned, and determining size or area.

To make this interpretation of "delay values" more explicit, Applicant amends claim 2 to clarify the term, in a manner consistent with the use of the terminology in the specification. The delay values are determined prior to placement, as stated in the claim, "as a function of delay to be provided by the corresponding cells and delay to be provided by loads on the corresponding cells." This matches the description of delay values throughout the specification. See for example the discussion of computation of delay values before placement (during library analysis in this example) on page 21 of the specification. Here, the specification describes delay values determined before placement using equation (1): "D = f(C/S)" on page 21, line 17, where C is a factor based on load, and S is a scale factor based on the cell. This function used to determine delay values for the cells is explained at page 21, lines 21-22, where the specification states: "The delay value depends on the delay provided by a cell plus the delay provided by the net (wire) load of the cell."

In the following, the Kannan *et al.* reference is discussed, as well as each of the claims at issue.

The basic process in Kannan *et al.* is shown in the flow on the right side of Fig. 2 in the reference, reproduced below.

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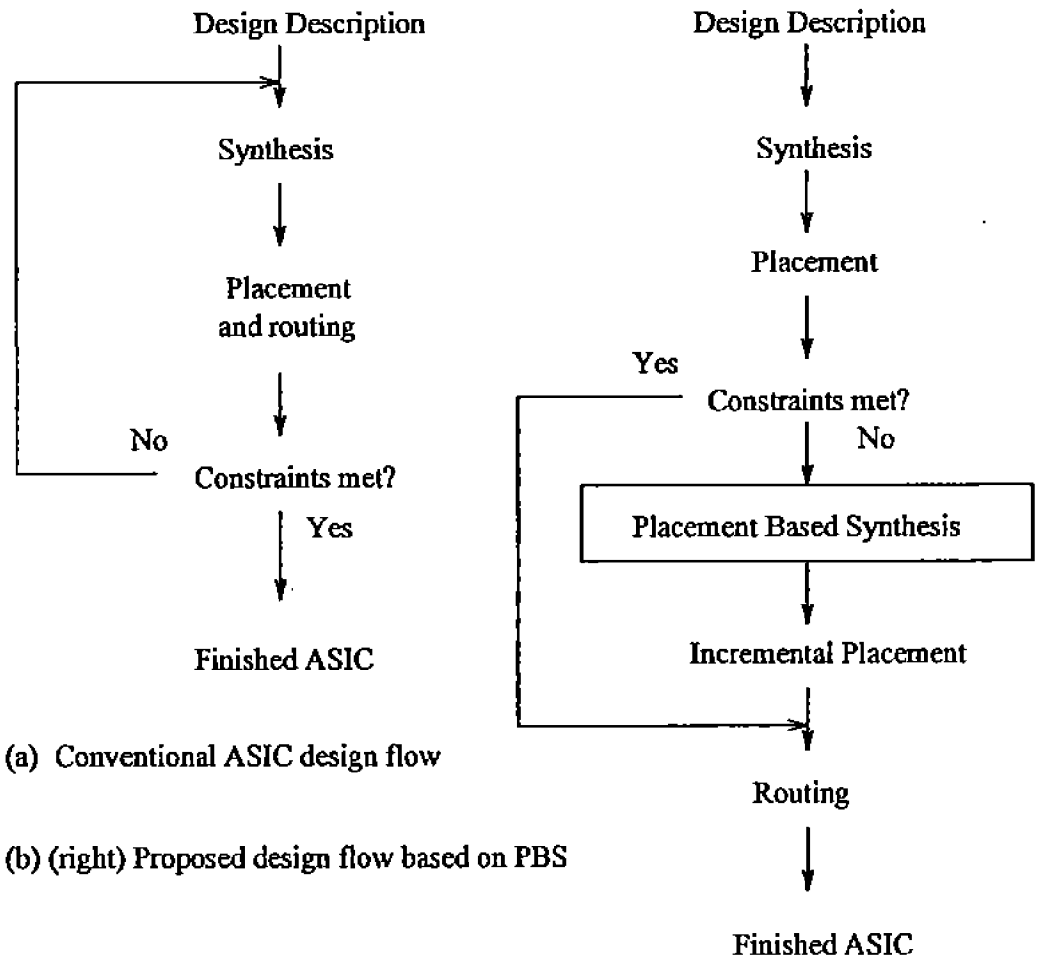


Figure 2: Comparison of ASIC Design Flows

Kannan *et al.*, page 328.

Kannan *et al.* determines delay values for cells after placement. Specifically, the "Constraints met?" step after placement determines delay values based on the combination of the cell and the load on the cell. Kannan *et al.* performs "placement-based timing analysis" which determines delay values after placement, to check timing constraints and to direct the "Placement Based Synthesis" step. See, Kannan *et al.*, p. 328, paragraph spanning the bottom of the first column to the top of the second column. The "Placement Based Synthesis" in Kannan *et al.* includes fanout buffering and gate-resizing, both of which depend only on delay values determined after placement by placement-based timing analysis.

The placement-based timing analysis is described in Section 2 of Kannan *et al.* The delay associated with the cell is based on an equation that considers intrinsic gate delay, load

delay due to the loading at the output pin, interconnect or wiring delay and input slew delay. See, Kannan *et al.* at the lower half of the second column of page 328. At least the load delay and the interconnect or wiring delay values are dependent in part on estimated wiring capacitance computed from placement locations. Accordingly, Kannan *et al. et al.* does not determine the delay values for cells prior to placement and *a priori* does not utilize such delay values as required by claim 2.

As to element (b) of claim 2, the Office position that the "determining delay values..." limitation of claim 2 is met by Kannan *et al.*, as follows:

> (b) determining delay values for with the selected plurality of cells in order to satisfy delay constraints (section 2 describes placement-based timing analysis including delay calculations of selected cells in order to satisfy delay constraints in placement-based delay optimization described in section 3, by a placement-based synthesis system described in section 4; for example, placement-based delay optimization include insertion of buffers at p0 and p3 in Fig. 5(b) to satisfy delay constraints; the buffer configuration meets the timing constraints as shown in Fig. 5(b), see section 3.1 page 330]; and

Office Action, page 3.

This passage does not take a position of what delay values are determined prior to placement, and in fact, there is no discussion in the reference of determining delay values before placement. The delay values utilized in the process of Kannan *et al.* are determined after placement.

The "insertion of buffers" example referred to in the just quoted statement from the Office Action is instructive of the point that Kannan *et al.* determines delay values only after placement. Specifically, Kannan *et al.* describes a process of fanout buffering, which is part of the placement-based delay optimization that is performed after placement. The fanout buffering process depends on first stripping off all of the buffers introduced by the original synthesis, in order to allow a "placement-based buffer insertion from scratch taking true wire parasitics into

account." Kannan *et al.*, page 329, second column. "True wire parasitics" are available only after placement.

The algorithm in pseudocode for fanout buffering is shown in Figure 6 of Kannan *et al.* This algorithm depends on computing slack represented in the pseudocode by the parameter $s_i$, at each node, and depends on the load at each node represented by the term $C_{T(i)}$ in the pseudocode. Both the slack at the node and the load at the node are values determined by placement, and are not determined before placement.

The Office alleges that element (c) of claim 2 is met by Kannan *et al.* by applying the "entire document." Office Action, page 4, line 6. The allegation of anticipation includes references to both the fanout buffering process and the gate resizing process described in the reference. However, there is no place in the reference at which placement is performed after determining delay values. There is no place in the reference in which size or area is determined in response to a delay value determined prior to placement and a load determined after placement.

The Office Action suggests mistakenly that the fanout buffering process includes a placement after determining delay values. Fanout buffering is a post placement process, relying on delay values determined after placement, which inserts buffers at predetermined places on the layout.

In the fanout buffering process, as discussed above, nodes p0 and p3 are defined among placed cells p1, p2, p4 and p5, as the "internal vertices of the minimal spanning tree" for interconnecting the cells. Buffers to be inserted must be placed at those vertices, and loads are determined based on that placement as described in the first column of page 330, in the paragraph on page 330 just beneath the Figure 5 of Kannan *et al.* Therefore, buffer insertion is performed after placement, and utilizes the information of that placement to compute the delay information used in the process.

As mentioned above, the pseudocode describing the fanout buffering relies on computation of delay values using the load at a placed node as represented by the term $C_{T(i)}$, after placement and not before. There is no mention of delay provided by the buffer itself.

Likewise, in the gate resizing process of Kannan *et al.*, delays are determined after placement. The gate resizing process depends on computation of the delay parameter known as slack at all of the affected nodes, using the data about the placed cell, the load delay and the

wiring delay determined during placement. The pseudocode for the gate resizing process is shown in Figure 8 of the reference. As in the pseudocode for fanout buffering, the parameter $s_i$ represents the slack value being analyzed. That delay parameter is determined according to Kannan *et al.* after placement. Therefore, the size or area of a cell is not set in Kannan *et al.* using delay values determined prior to placement and the load assigned during placement, as required in the claim.

Accordingly, the position in the Office Action that claim 2 is anticipated by Kannan *et al.* is mistaken. Specifically, the delay values utilized in the fanout buffering process and in the gate resizing process of Kannan *et al.* are determined after placement. Also, there is no process in Kannan *et al.* for determining size or area that takes into account both the delay values determined before placement and the loads assigned during placement. For these reasons, claim 2 is not anticipated, and withdrawal of the rejection is requested.

With regard to claim 5, the Office Action also takes the position that the reference describes the step of "determining the size or area of the cells that will approximately maintain delay values determined prior to placement." As explained above, Kannan *et al.* determines delay values after placement. Therefore, there is no process of determining the size or area of cells using values determined prior to placement described in the reference.

The position in the Office Action concerning claim 5 refers to the fanout buffering process. The fanout buffering process in Kannan *et al.* discards all of the buffers in the original net list after the placement process. There are no delay values determined prior to placement, associated with either the discarded buffers or the new buffers at the time the fanout buffer processing is executed. It would be impossible therefore to determine size or area of the buffers to "maintain said delay values determined prior to placement," using the fanout buffering process of Kannan *et al.* The buffers selected prior to placement in Kannan *et al.* have been discarded. It does not make sense to assert that inserting new buffers from scratch, as taught by the reference, is the same as determining a size of a buffer that has been removed from the circuit.

Claim 7 is dependent on claim 2. It distinguishes over the references for at least the same reasons as claim 2 discussed above.

Claim 8 states that the delay values, determined before placement, are determined using gain. The Office Action refers to the delay computation in the reference which depends on information that is determined by placement. Accordingly, the position of the Office Action is

clearly mistaken. Furthermore, the term "gain" is clearly defined in this specification as the ratio of output capacitance to input capacitance: $C_{out}/C_{in}$, See Fig. 9A of the present specification for example. Accordingly, the position taken in the Office Action is based on an interpretation of the term "gain" which is inconsistent with the specification.

Claim 9 states that the delay values, determined before placement, are determined using logical effort. The Office Action refers to a section of Kannan *et al.* describing "placement-based timing analysis." In Kannan *et al.*, placement-based timing analysis is performed after placement. Accordingly, the position of the Office Action is clearly mistaken. Furthermore, the position taken in the Office Action is based on an interpretation of the term "logical effort" which is inconsistent with the specification.

Claim 10 requires determining delay values by finding a preferred gain. Claim 10 distinguishes for at least the same reason as claim 8. The reference does not discuss any computation based on the parameter "gain" as properly interpreted in light of the present specification.

Claim 11 depends on claim 10, and is patentable for at least the same reasons.

Claim 12 depends from claim 2, and is patentable for at least the same reasons. Furthermore, the claim is rejected based on a characterization that the post-placement delay optimization described in the reference is a "library analysis." Applicant submits that this interpretation of the term "library analysis" is inconsistent with the present specification. Also, post-placement delay optimization cannot perform the step recited in claim 12, as it depends from claim 2, which requires determining delay values prior to placement.

Claim 13 depends from claim 2, and is patentable for the same reasons. Furthermore, applicant submits that the Examiner is mistaken in characterizing the post-placement delay analysis as based on "typical load." Rather, the delay analysis in Kannan *et al.* is based on information determined during placement, and is therefore executed after placement.

Claim 14 depends from claim 13, and is patentable for at least the same reasons. Again, claim 14 requires determination of a typical load based on gain considerations. There is no process in the reference which utilizes the parameter "gain" as properly interpreted in light of the present specification.

Claim 15 depends from claim 2, and is patentable for at least the same reasons. Furthermore, the process of the gate resizing described in the reference does not depend on the size or areas of cells in a placed circuit being variable as required by the claim.

Claim 16 is an independent claim which requires "determining initial delay values... before determining an initial size or area of the cells" and "performing an initial placement of the cells... and determining the initial size or area of the cells in response to the initial placement." It is impossible for the reference to achieve the step of determining initial delay values before determining initial size or area, because the reference depends on the intrinsic delay of the cell and on delay parameters that are due to the placement of the cell, to calculate a delay value. The intrinsic delay of the cell is only known when the size or area of the cell is known. Therefore, the rejection of claim 16 is based on a mistake in fact, and should be withdrawn.

Claim 17 depends from claim 16 and is patentable for at least the same reasons. Likewise, claim 18 depends from claim 16 and is patentable for at least the same reasons.

Accordingly, reconsideration of the rejection of claims 2, 5 and 7-18 as amended is respectfully requested.

## CONCLUSION

It is respectfully submitted that this application is now in condition for allowance, and such action is requested.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (SYNP 1006-0).

Respectfully submitted,

Dated: 15 December 2009 /Mark A. Haynes/

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